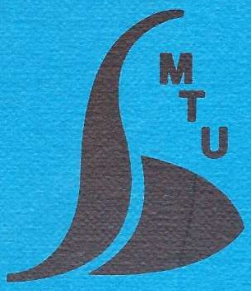

Micro
Technology
Unlimited

K-1016 16K BYTE MEMORY

6502 SYSTEM
LOW POWER MEMORY

JANUARY 1, 1979 REVISED SEPTEMBER 5, 1979

1979

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K-1016 UNPACKING AND INSTALLATION

The K-1016 16K Memory is a carefully engineered, manufactured, and tested product that should operate perfectly when handled and installed according to the following instructions. Note that the board is shipped in a black conductive plastic bag. Since MOS integrated circuits are used, damage from static discharge is possible. It is helpful to reduce static by working in an area with concrete floors and a reasonable humidity level. If this is impossible, at least avoid wearing rubber soled shoes and move slowly in the work area. When unpacking or handling the board, touch the screw sticking up in the middle of the heatsink first and release it last. Note that the preceeding comments apply equally to the KIM-1 board which contains MOS IC's also.

ADDRESS SELECT JUMPERS Jumper socket S1 is shipped with jumpers installed for board addressing between 4000 and 7FFF. If at all possible, the board should be tested in the user's system with these jumpers intact. Following testing, they may be reconfigured as desired according to the table below:

ADDRESS RANGE	JUMPERS BETWEEN PINS			ADDRESS RANGE	JUMPERS BETWEEN PINS			
0000-3FFF	1-8	4-5		7000-AFFF	1-8	3-6		
1000-4FFF	2-7			8000-BFFF	1-8	3-6	4-5	
2000-5FFF	2-7	4-5		9000-CFFF	2-7	3-6		
3000-6FFF	1-8	2-7		A000-DFFF	2-7	3-6	4-5	
4000-7FFF	1-8	2-7	4-5	B000-EFFF	1-8	2-7	3-6	
5000-8FFF	3-6			C000-FFFF	1-8	2-7	3-6	4-5
6000-9FFF	3-6	4-5						

If desired, the user may install a DIP header wired with the jumpers or a standard 4 pole dipswitch into S1.

POWER SUPPLY REQUIREMENTS Note that as shipped the board requires an unregulated voltage between +7 and +12 volts to operate the logic and another unregulated voltage between +14 and +20 volts to operate the memory chips such as provided by the expansion outputs of an MTU K-1000 power supply. The on-board regulators may be bypassed by shorting the two outside pins of each regulator IC together if the user wishes to use a regulated power source. When used with the K-1007 PET interface the necessary power requirements have already been taken care of and need cause no concern.

CONNECTION TO USING SYSTEM Connection to the using system should be as indicated in the accompanying table. The easiest method of connection to KIM/SYM/AIM processors is with an MTU model K-1005 motherboard and cardfile. Alternatively the user may obtain two double-sided 22 pin printed circuit board edge connectors (.156" contact spacing) such as the one supplied with the processor and wire them together except for contacts 2, 3, 16-20, and X. Wire length should not exceed 4 inches and the ground wire (pin 22) should be #16 gauge or heavier. KIM-1 users will also have to connect the VECTOR FETCH signal (pin 19) to pin J on the KIM application connector and DECODE ENABLE (pin 20) to pin K on the KIM application connector.

Next make the necessary power connections to the socket intended to receive the K-1016 and plug in the K-1016. Plug the processor into the other socket. PET users with the K-1007 should simply plug the K-1016 into the socket on the K-1007 board with the component side of the K-1016 pointing away from the K-1007. If another MTU board is already being used with the K-1007, a K-1005-PET card file/motherboard will have to be used to hold the multiple boards.

TESTING After connecting the processor and the power supply, the system may be turned on. Pressing RESET on the processor should initiate normal operation. Set the address to 4000 and store different values there. Repeat at 5000, 6000, and 7000 so that each row of memory chips is tried. The processor data display should be stable and reflect the data stored (the AIM should not indicate a memory error).

If all is well at this point the test program supplied with the K-1016 should be loaded through the processor keyboard and dumped to cassette tape. The entry point is 0200 and the return jump to the monitor should be modified if a board other than the KIM is being used. The test program generates a sequence of completely random bytes and stores them in memory in a scrambled order based on a random number. Following the store phase, the same pattern and order is regenerated and compared with memory contents. If comparison is successful, another test cycle with a different pattern and different store order is executed. Every 16 test cycles a 15 second delay is inserted between the store and verify phases to insure that memory refresh is working. The program should run indefinitely without stopping. If it does stop, locations 0000 and 0001 indicate the address of the failure and address 0002 shows the bit or bits in error. PET users should modify the BASIC test program included with the K-1007 manual to test 16K of memory. At this point checkout of the K-1016 is complete.

SPECIFICATIONS

Access Time - Greater than 100NS data stable time prior to fall of system phase 2 clock

Cycle Time - Internally synchronized to 1 mHz system phase 2 clock.

Memory Type - 22 pin dynamic, high level clock (National MM5280 or equivalent)

Buffering - - Maximum of 1 LS TTL load on address and data bus

Power - - - - +7.5 volts unregulated 0.2 amp, +16 volts unregulated 75 milliamp standby, 200 milliamp maximum with 100% access.

Addressing - The 16K must be contiguous, starting at any 4K boundary. An 8-pin IC socket is provided for jumpers.

Adjustment - phase locked loop synchronization for timing generator, factory set.

Sockets - - - The 32 memory IC's and address jumpers are socketed.

PC Board - - 11 inches wide 7.5 inches tall exclusive of gold plated edge connector, plated through holes.

Inclusions - Bare or assembled and tested board, instruction manual containing schematic, trouble-shooting tips, and memory diagnostic.

BUS STANDARD PIN CONNECTIONS

PIN	KIM-1	SYM-1	AIM-65		MTU
E-1	SYNC	SYNC	SYNC		SYNC
E-2	RDY	RDY	RDY	* #	VM VIDEO
E-3	PHASE 1	PHASE 1	PHASE 1		PHASE 1
E-4	IRQ	IRQ	IRQ		IRQ
E-5	SET OVERFLOW	SET OVERFLOW	SET OVERFLOW		SET OVERFLOW
E-6	NMI	NMI	NMI		NMI
E-7	RESET	RESET	RESET		RESET
E-8	DATA BUS 7	DATA BUS 7	DATA BUS 7		DATA BUS 7
E-9	DATA BUS 6	DATA BUS 6	DATA BUS 6		DATA BUS 6
E-10	DATA BUS 5	DATA BUS 5	DATA BUS 5		DATA BUS 5
E-11	DATA BUS 4	DATA BUS 4	DATA BUS 4		DATA BUS 4
E-12	DATA BUS 3	DATA BUS 3	DATA BUS 3		DATA BUS 3
E-13	DATA BUS 2	DATA BUS 2	DATA BUS 2		DATA BUS 2
E-14	DATA BUS 1	DATA BUS 1	DATA BUS 1		DATA BUS 1
E-15	DATA BUS 0	DATA BUS 0	DATA BUS 0		DATA BUS 0
E-16	K6	30	-12 VOLTS REG.	* #	VM HORIZ SYNC
E-17	SINGLE STEP OUT	DB OUT	+12 VOLTS REG.	* #	VM VERT SYNC
E-18	(N.C.)	POWER ON RESET	CS8	* #	+7.5 UNREG
E-19	(N.C.)	(N.C.)	CS9	*	VECTOR FETCH
E-20	(N.C.)	(N.C.)	CSA	*	DECODE ENABLE
E-21	+5 VOLT REG.	+5 VOLT REG.	+5 VOLT REG.		+5 VOLT REG.
E-22	GROUND	GROUND	GROUND		GROUND
E-A	ADDR BUS 0	ADDR BUS 0	ADDR BUS 0		ADDR BUS 0
E-B	ADDR BUS 1	ADDR BUS 1	ADDR BUS 1		ADDR BUS 1
E-C	ADDR BUS 2	ADDR BUS 2	ADDR BUS 2		ADDR BUS 2
E-D	ADDR BUS 3	ADDR BUS 3	ADDR BUS 3		ADDR BUS 3
E-E	ADDR BUS 4	ADDR BUS 4	ADDR BUS 4		ADDR BUS 4
E-F	ADDR BUS 5	ADDR BUS 5	ADDR BUS 5		ADDR BUS 5
E-H	ADDR BUS 6	ADDR BUS 6	ADDR BUS 6		ADDR BUS 6
E-J	ADDR BUS 7	ADDR BUS 7	ADDR BUS 7		ADDR BUS 7
E-K	ADDR BUS 8	ADDR BUS 8	ADDR BUS 8		ADDR BUS 8
E-L	ADDR BUS 9	ADDR BUS 9	ADDR BUS 9		ADDR BUS 9
E-M	ADDR BUS 10	ADDR BUS 10	ADDR BUS 10		ADDR BUS 10
E-N	ADDR BUS 11	ADDR BUS 11	ADDR BUS 11		ADDR BUS 11
E-P	ADDR BUS 12	ADDR BUS 12	ADDR BUS 12		ADDR BUS 12
E-R	ADDR BUS 13	ADDR BUS 13	ADDR BUS 13		ADDR BUS 13
E-S	ADDR BUS 14	ADDR BUS 14	ADDR BUS 14		ADDR BUS 14
E-T	ADDR BUS 15	ADDR BUS 15	ADDR BUS 15		ADDR BUS 15
E-U	PHASE 2	PHASE 2	PHASE 2		PHASE 2
E-V	READ/WRITE	READ/WRITE	READ/WRITE		READ/WRITE
E-W	READ/WRITE	READ/WRITE	READ/WRITE		READ/WRITE
E-X	PLL TEST	AUDIO TEST	AUDIO TEST	* #	+16 VOLT UNREG.
E-Y	PHASE 2	PHASE 2	PHASE 2		PHASE 2
E-Z	RAM R/W	RAM R/W	RAM R/W		RAM R/W

* = This signal IS NOT bussed to the CPU slot on KIM, SYM, or AIM versions of the K-1005 card file.

= This signal IS bussed to the CPU (top) slot on the PET versions of the K-1005 card file.

PRINCIPLES OF OPERATION

The K-1016 16K dynamic memory uses several innovative design techniques to simultaneously achieve high reliability, totally transparent refresh, low power consumption, and complete KIM/VIM/AIM compatibility. Standard 22 pin 4K dynamic RAM's are utilized to provide the optimum combination of low cost, low power consumption, minimum support circuitry and multiple sources of supply. As stated above, refreshing is done in a manner that does not affect the operation of the 6502 processor at all. Therefore from the user's point of view, the board acts like a static memory board but with the cost and power advantages of dynamic boards.

BASIC BOARD TIMING The key to the board's remarkable properties is the 6502 bus itself. A symmetrical 1.0 mHz two-phase clock is used by the 6502. The 6502 microprocessor really accesses memory only during Phase 2 with Phase 1 being used for setup. Thus the K-1016 memory can use the 500NS period during Phase 1 to refresh the memory and then turn the memory over to the 6502 during phase 2. RAM chip access times approaching 300NS are required with this scheme but that figure is actually rather slow compared with modern 4K dynamic RAM standards. It is this "flip-flop" sharing between microprocessor and refresh that allows totally transparent refresh action under all operating conditions.

MEMORY ARRAY The memory array itself consists simply of 32 4K dynamic RAM chips of the 22 pin variety arranged in a 4 by 8 array. The primary reason for their use over other types of memory chips was cost and a long history of trouble-free reliable performance in large mainframe computers. Also they have the lowest average power consumption in this circuit of all available 4K RAM's. Although National Semiconductor MM5280's are used on factory assembled boards, many manufacturers produce compatible products. Exact details on the operation of 22 pin 4K dynamic RAM's may be found in the manufacturer's data sheets.

MEMORY CHIP CLOCK One signal required by the RAM chips is a clock signal that is 12 volts in amplitude. The leading edge of this signal causes the RAM's themselves to latch the state of the address inputs and hold it until clocked again. Data appears at the output after access time, which is typically 200NS, and remains until the clock returns to ground. When not clocked, the RAM's remain completely inactive, draw no power, and float their outputs. A power saver circuit generates a clock pulse only when a memory cycle is actually needed and only clocks the row of RAM's that was actually addressed. At all other times the memory array draws no power at all. If the processor is not accessing the board, less than 17% of the possible memory cycles are active which rises to about 67% if the 6502 is in a tight loop fetching and executing solely on the 16K board. An individual RAM chip will see from 1/4 to over 3/4 of this activity level depending on what the program is doing. The result is that the memory array runs from stone cold when the program is executing elsewhere to just cold when fully utilized.

BUS CLOCK SYNCHRONIZATION All of the board's timing is derived from an 8mHz oscillator which is phase-locked to the rising edge of PHASE 2 from the 6502. Each cycle of this oscillator represents a time slot for the timing generator which is 125 NS. U45 is the voltage controlled oscillator in the phase locked loop which is just a classic Schmidt trigger R-C oscillator. The 500 ohm pot (P1) determines the oscillator's free-running frequency and is set for a nominal frequency of 8.0mHz. This simple oscillator is made to act as a voltage controlled oscillator (VCO) by connecting a resistor (2.2K, R18)) to the R-C node. Changes in current through this resistor caused by voltage changes at its free end affect the oscillator's frequency. Although the linear VCO range is only 20% or so, this is ample for locking to the fixed crystal-controlled frequency of the using processor.

PHASE DETECTOR The phase detector is also rather unique. Since the phase angle of the lock between the on-board oscillator/counter chain and the 6502's PHASE 2 clock affects the data transfer timing, it had to be controlled more tightly than a typical exclusive-or phase detector would provide. A tri-state buffer (U46) fills the bill. A 125NS pulse at a 1.0mHz rate from the first three stages of the counter chain enables the tri-state buffer. The data input to the buffer is PHASE-2 from the processor. Ideal timing for data transfer between processor and K-1016 occurs when the trailing edge of PHASE 2 occurs midway in the enable pulse. Under these conditions the output of the buffer floats for 7/8 of the cycle, is driven high for about 1/16 of the cycle, and then is driven low for the remaining 1/16 of the cycle before floating again. This wildly gyrating buffer output voltage is averaged by the low pass filter formed by R15 and C1. If PHASE 2 turns off earlier in the enable window, the buffer output high time becomes less than the low time and the low-pass filter output voltage decreases thus speeding up the VCO which corrects for the error. The converse is true if PHASE 2 becomes late. The exact equilibrium point can be changed by adjusting the 500 ohm pot, P1.

TIMING GENERATOR The 8mHz signal from the PLL next enters U33 which is a 4 bit binary counter. The first 2 stages function as a divide by 4 and time individual memory cycles which are actually 500NS long. The important output from the first two counter stages however is the MEM CE signal which controls the critical "chip enable" clock to the memory chips. As shown in the timing diagram, MEM CE is true for 5/2 of the 8mHz signal (313NS) and false for the other 3/2 (187NS). These times may vary slightly according to the 8mHz waveform symmetry but are far more stable than a single-shot timing generator would be.

The third stage of U33 awards even numbered memory cycles to the 6502 and odd numbered ones to the refresh logic. This function is exercised via the signal SEL KIM ADDR. The last stage of U33 and a portion of U35 are set up to actually allow a refresh cycle on every fourth refresh oppertunity. This minimizes power consumption from excessive refreshing while allowing a complete memory refresh every millisecond. U34-8 is the gate that detects refresh cycles divisible by 4. U17 generates the 125NS enable pulse for the phase detector at the proper time with respect to the other signals.

REFRESH ADDRESS GENERATOR The refresh address counter is 8 bits long and consists of U31. At the end of an actual refresh cycle, the counter increments by one in preparation for the next refresh cycle. In order to minimize noise, the 12 volt clock to the RAM chips is fully decoded thus only 8 RAM's are clocked on any one cycle. This decoding extends to refresh also simplifying the clock circuitry and preserving low noise during refresh cycles. Most other dynamic memory boards cannot afford the extra refresh time this technique costs but with a million opportunities for refresh every second on the K-1016, it is a very viable technique. The lower 6 bits of the refresh address counter address the 64 rows of the RAM's chips which must be refreshed. The remaining two bits address the four rows of RAM chips one at a time for refreshing.

REFRESH ADDRESS MULTIPLEXOR An 8 bit 2 input address multiplexor is formed from U20 and U32. This multiplexor selects addresses from the refresh address counter when SEL KIM ADDR is false and selects addresses from the 6502 when it is true. SEL KIM ADDR is roughly the inverse of KIM PHASE 2 but occurs about 50 to 100 NS earlier. U8 functions as a partial multiplexor for the remaining 4 RAM address bits by providing an unconditional high output when SEL KIM ADDR is false. The output of the address multiplexor drives the 12 address lines of the RAM array directly. Normally this would not be enough power to absorb the address line noise that occurs when the RAM's are clocked but since no more than 8 are clocked at once, they are quite adequate. U30 multiplexes three additional signals between the KIM and the refresh logic. Two of these are simply the two most significant address bits. The third is a signal that indicates whether a memory cycle is really needed. On the processor side a cycle is only needed if the board is addressed. On the refresh side only every fourth cycle is needed.

CLOCK DRIVER The clock driver circuit that accepts TTL levels from U36 and translates them to 12 volt levels is exceptionally simple, cheap, power conservative, and high in performance. Like the RAM array, the clock driver draws no power except when a clock pulse is being generated. Performance of the circuit when loaded by 8 RAM chips rivals that of $3 driver IC's with rise and fall times of less than 25NS. When the TTL level input goes positive, the NPN transistor saturates causing a low output level. The same edge creates a reverse voltage pulse through the 220PF capacitor which quickly turns the PNP off. When the TTL input goes negative the NPN turns off while a negative pulse of current through the 220PF capacitor turns the PNP on thus forcing the output to +12 volts. Since the load on the clock driver is purely capacitive, the PNP need not continuously pull the output up hard for the entire pulse width. The 100PF capacitor serves to speed up the NPN turnoff.

PROCESSOR BUS INTERFACE Looking now at the processor side of the interface, U6 and U7 buffers the upper 8 address bus bits and provides them in true form while part of U18 provides A13-A15 in complement form as well. These complement address bits in conjunction with a gate from U17 detects address references between 0000 and 1FFF and generates KIM DECODE ENABLE to allow the KIM monitor ROM's to function when A-K is disconnected from ground (this signal is not needed by other 6502 processors). An 8-input nand gate, U19, detects references between FF00 and FFFF and generates KIM VECTOR FETCH. A germanium diode in series with the gate output simulates the open-collector gate which is required.

ADDRESS RECOGNITION The board address recognition circuitry is a bit strange to allow addressing the 16K memory on any 4K boundary. U5 is actually a 4 bit binary adder. This IC performs a 4 bit addition of its B inputs, which are the upper 4 bits of the KIM generated address, and its A inputs which are tied to 4 jumpers. The sum which appears at the outputs is the actual binary sum of the inputs. If overflow beyond 15 occurs, the sum output is modulo 16 of the real sum. The lower 2 bits of the sum select a row of RAM chips while the upper two bits activate BOARD ADRD only if they are both ones. Thus in order for the board to respond to an address, the sum of its upper 4 bits and the binary value of the jumpers must be between C and F (hexadecimal).

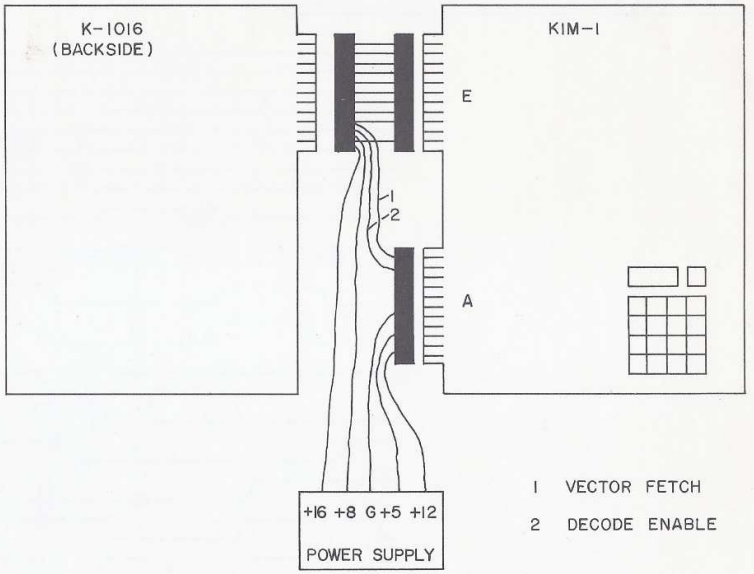
DATA BUS BUFFERS The processor data bus is buffered both to and from the actual RAM array. Data from the bus passes through U1 and U3 on its way to the RAM DATA INPUT pins. The inversion of the data is cancelled by the data inversion inside the RAM itself. Data output from the RAM enters a tri-state latch which is necessary because data from the RAM's has disappeared by the time the 6502 uses it. The latches have new data clocked into them at the end of every memory cycle but their contents are gated onto the processor data bus only when the board is addressed and a write cycle is not being performed.

WRITE ENABLE SIGNAL A portion of U34 generates the write enable signal to the RAM array. This signal is coincident with the RAM chip enable clock and is generated only when the board is addressed, a 6502 cycle is being executed, and write enable is present on the bus. Since only one row of RAM chips is actually clocked, the write enable signal can be distributed to all 32 RAM's in parallel.

POWER SUPPLY REGULATORS Two 3-terminal regulators supply regulated +5 and +12 volts from unregulated input voltages. Minimal heatsinking is necessary due to the low power consumption of the board. The 1000uF filter capacitor on the +16 unregulated input allows the K-1000 power supply to power up to 48K of K-1016 memory as well as a KIM and K-1002 DAC all simultaneously. Typically a K-1008 Visible Memory can be added in also making for a really powerful system that runs on less than 25 watts of power. Negative 5 for the RAM chips is supplied by a charge pump and zener diode regulator. Two sections of U29 in parallel provide a 12 volt P-P signal at 1mHz which drives the network consisting of CR2, CR3, CR4, C70 and C109 which, without CR4, would produce about -11 volts. CR4 reduces this to -5 volts and in doing so limits the swing at U29-11 and 3 to about 6 volts P-P.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

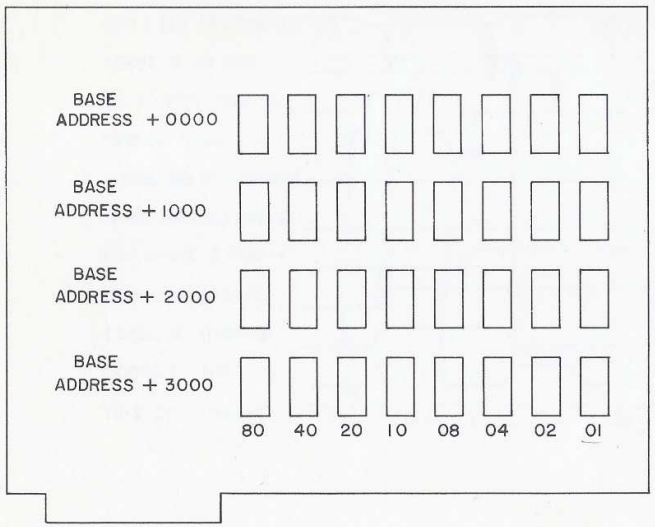
PARALLEL BUS
EXCEPT PIN X



1 VECTOR FETCH

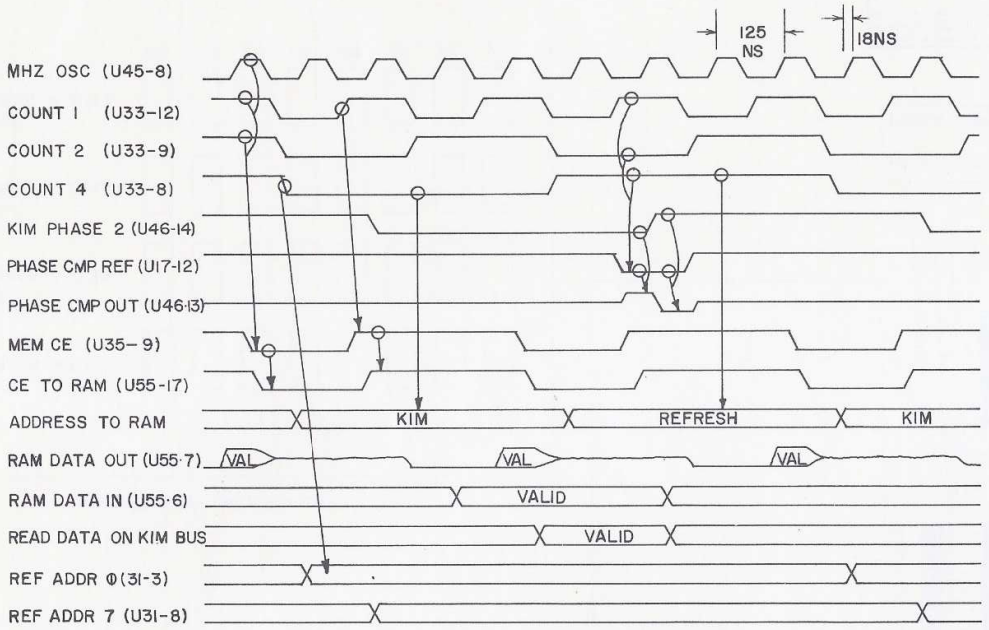
2 DECODE ENABLE

MEMORY CHIP DATA BIT MAP



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS ± DEC. ± ANGLES ±		MICRO TECHNOLOGY UNLIMITED	
APPROVALS	DATE	K-1016 BIT MAP & CONNECTION	
DRAWN DBC	1-3-79		
CHECKED		SCALE	SIZE B / DRAWING NO.
		DO NOT SCALE DRAWING	SHEET 1-1

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED



TOLERANCES UNLESS OTHERWISE SPECIFIED FRACTIONS DEC. ANGLES ± ± ±		MICRO TECHNOLOGY UNLIMITED	
APPROVALS	DATE	K-1016 MEMORY TIMING	
DRAWN DBC	12-78		
CHECKED		SCALE	SIZE B / DRAWING NO.
DO NOT SCALE DRAWING			SHEET 1-1

TROUBLESHOOTING GUIDE

In the event that your K-1016 does not work properly, the following suggestions should be tried before returning the board to the factory for repair. This is to the customer's benefit since shipping delays alone often amount to two weeks even if the repairs are made immediately upon receipt at the factory.

If the processor display is unstable when reading any location within the address range of the board check your power supply. Although unregulated input voltages are expected, the DC voltage minus the ripple must not be less than 14 volts and 7 volts for the memory and logic supplies respectively. If a voltmeter indicates less than 15 and 8 volts be suspicous. Try a larger filter capacitor in the power supply. If it makes any difference then that is the problem area. If the on-board regulators are bypassed, make sure that the supply voltages measured at the IC pins are within 4% of +12 and +5 and that ripple is less than 50 millivolts peak-to-peak.

If the supply voltages are OK then it is possible that the PLL adjust potentiometer on the board has drifted or been tampered with. Rotate the pot both ways until the data display is stable when examining a memory location on the K-1016 board. If a multimeter is available, further rotate the pot until a voltage reading at U46 pin 13 of 1.4 volts is achieved. The processor's display should remain stable. If a meter is not available, note the extremes of rotation that provide a stable display and set the pot midway between the extremes. A spot of nail polish will serve to prevent future drifting of the adjustment.

Check the clock waveform to the RAM chips, it should be a full 12 volts in amplitude and have 25NS or less transition times. The top and bottom of the waveform should be reasonably flat with ringing less than 1V P-P. Use a short ground connected directly between the probe and emitter of the NPN clock driver transistor for checking this. If one of the clock driver transistors is bad, replace with the identical number.

If the test program fails and consistantly points out the same bit in the same 4K block of memory addresses then it is likely that a RAM chip is bad. Prior to shipment the board was continuosly checked with a similar program for 24 hours and no memory errors were allowed. Consult the accompanying chart to determine which RAM is bad and carefully remove it from the socket. Virtually any 22 pin 4K dynamic RAM with high-level clock and a 300NS access/470NS cycle speed may be substituted. Examples are MM5280 (NSC), TMS4060 (TI), 2107A, 2107B (Intel), 2604 (Sig.), and 9060 (AMD). Numbers to avoid are 2107 plain and TMS4030. Also if parts are being obtained to populate a blank board it is recommended that 2107B and TMS4060 with date codes prior to 1978 also be avoided.

Most other failures will require sharp eyes or an oscilloscope to trace. First examine the board underside to verify that unclipped excess component leads have not bent and shorted lines together. Also check the -5 supply voltage across D4; it should be between -4.5 and -5.5 volts.

Tracing with an oscilloscope is best done by checking the counter chain first. Look at the 8 MHz oscillator output and the first 3 counter stages. Then look at the phase comparator output. Adjust the pot until waveforms like the diagram are seen. Check the remainder of the counter chain and verify that REF EN occurs every 4uS. MEM CE should repeat at a 2 MHz rate and be high for approximately 315nS and low for 185uS.

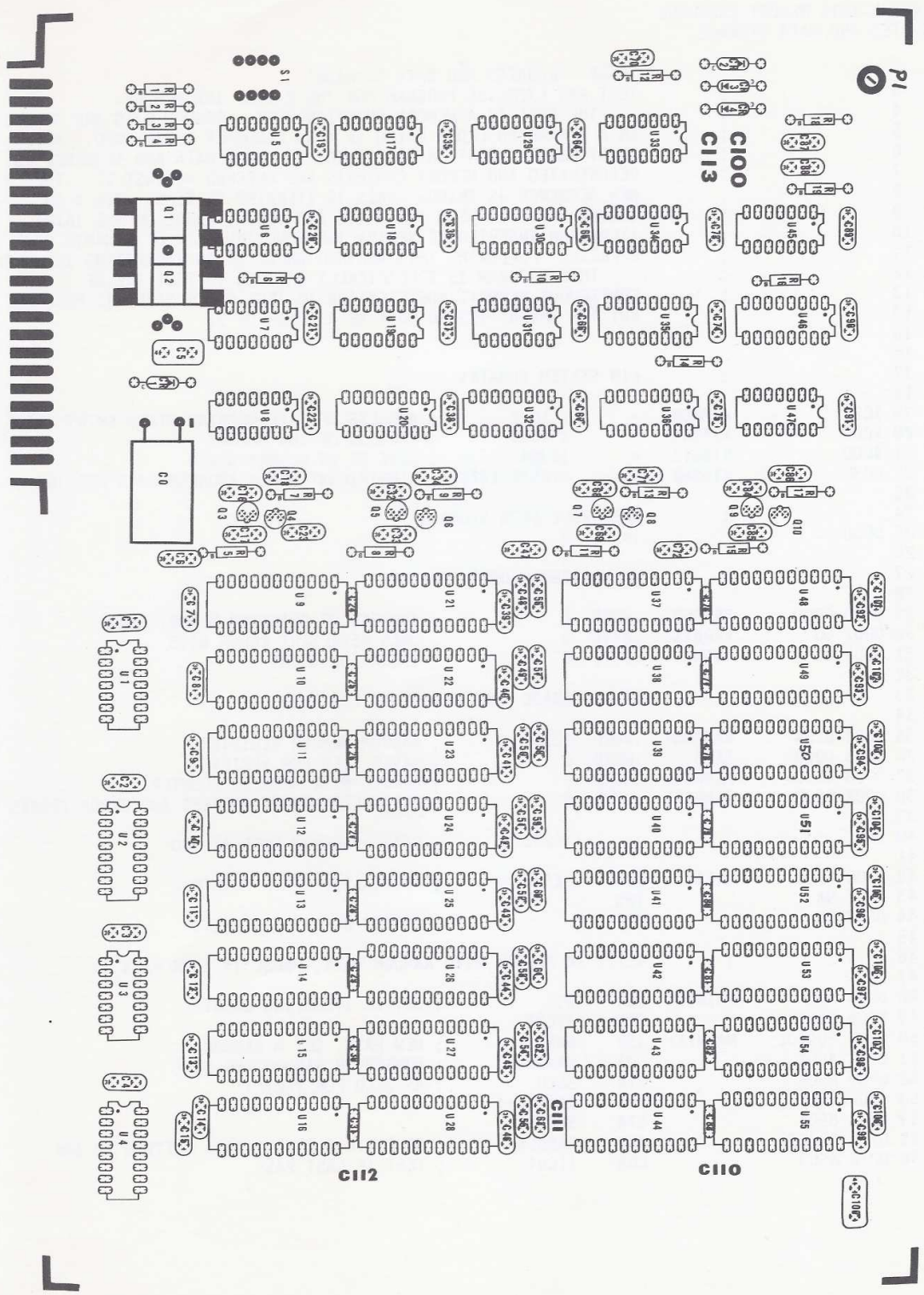
The refresh address counter chain should be checked next. Check that every bit is counting. Check the address multiplexor for proper functioning of each bit. With the KIM examining a location outside the address range of the board, the CE signal to any row of memory chips should be in groups of 64 pulses, the pulses 4uS apart and the groups 1.024mS apart. The pulse groups are staggered for each row.

With a program loop continuously reading a location on the board, synchronize the scope to board addressed (U29-8). Check that the data register is being gated onto the processor bus at this time. Check the RAM data outputs, they should be stable just prior to data register clocking which occurs 100-150nS before the end of phase 2.

If all of this fails to locate the problem, return the board to the factory.

PARTS LIST FOR K-1016
16K MEMORY

DESCRIPTION	QUANTITY	DESIGNATION	
LOGIC 74LS00	2	U8,47	
LOGIC 74LS04	3	U1*,3*,18	(*) MUST BE 74LSXX
LOGIC 74LS08	2	U6*,7*	
LOGIC 74LS10	1	U17*	
LOGIC 74LS13	1	U45	
LOGIC 74LS20	1	U34	
LOGIC 74LS26	1	U29	
LOGIC 74LS30	1	U19*	
LOGIC 74LS42	1	U36	
LOGIC 74LS93	1	U33	
LOGIC 74LS109	1	U35	
LOGIC 74LS158	3	U20*,30,32*	
LOGIC 74LS173	2	U2*,4*	
LOGIC 74LS283	1	U5	
LOGIC 74LS368	1	U46	
LOGIC 74LS393	1	U31*	
4K 22 PIN RAM CHIP	32	U9-16,21-28,37-44,48-55	
DIODE GERMANIUM 1N270	1	CR1	
DIODE SILICON 1N914	2	CR2,3	
DIODE ZENER 5.1V .4W	1	CR4	
TRANSISTOR 2N3646	4	Q3,5,7,9	
TRANSISTOR 2N4916	4	Q4,6,8,10	
VOLT REG. LM340T-5	1	Q1	
VOLT REG. LM342P-12	1	Q2	
CAP NPO 12V 68PF	1	C88	
CAP X7R 100PF 12V	4	C17,33,69,85	
CAP X7R 220PF 12V	4	C16,32,68,84	
CAP Z5U .01UFD 12V	2	C70,87	
CAP Z5U .047UFD 12V	105	C1-4,6-15,18-31,34-67,71-83,89-108,110-113	
CAP ELECT 100UFD 16V	3	C5,109,100	
CAP ELECT 1000UFD 25V	1	C0	
RES 1/4W 5% 270 OHM	1	R16	
RES 1/4W 5% 470 OHM	1	R19	
RES 1/4W 5% 1K	8	R5,6,8,10,11,12,14,15	
RES 1/4W 5% 2.2K	5	R7,9,13,17,18	
RES 1/4W 5% 10K	4	R1-4	
TRIMPOT 500 OHM	1	P1	
SOCKET 8 PIN PC	1	S1	
SOCKET 22 PIN PC	32	XU9-16,21-28,37-44,48-55	
SOCKET 14 PIN PC	1	XU19	
PC BOARD	1	PCB K-1016	
HEATSINK	1	H1	
SCREW,4-40X1/2 RH	1	MOUNT HEATSINK	
NUT,HEX,4-40X.250	1	MOUNT HEATSINK	
WASHER,FIBRE	1	UNDER HEATSINK	


P1
C100
C113
C111
C110
C112

```
                                .PAGE  'EQUATES AND DATA STORAGE'
    3                   ;       TEST AND EXERCISE PROGRAM FOR THE K-1016 16K MEMORY.
    4                   ;           THE TEST IS A MEMORY FUNCTION TEST.  RANDOM BITS ARE STORED
    5                   ;       IN A SCRAMBLED ORDER WHICH IS ALSO RANDOMLY DETERMINED.  AFTER
    6                   ;       EVERY MEMORY LOCATION IS FILLED, THE SAME DATA AND SEQUENCE IS
    7                   ;       REGENERATED AND MEMORY CONTENTS ARE CHECKED AGAINST IT.  THEN A
    8                   ;       NEW SEQUENCE IS TRIED.  THIS IS ITERATED 16 TIMES WITH A 16
    9                   ;       SECOND PAUSE BETWEEN THE WRITE AND VERIFY PHASE OF THE 16TH
   10                   ;       ITERATION INSERTED TO VERIFY THE FUNCTIONALITY OF DYNAMIC RAM
   11                   ;       REFRESH.  FOLLOWING THIS ANOTHER GROUP OF 16 ITERATIONS IS DONE
   12                   ;           THIS PROGRAM IS SPECIFICALLY WRITTEN TO TEST 16K OF
   13                   ;       CONTIGUOUS MEMORY. MODIFICATION TO TEST OTHER SIZES IS POSSIBLE
   14                   ;       BUT THE AMOUNT TESTED MUST BE A POWER OF 2.
   15
   16
   17                   ;       KIM SYSTEM EQUATES
   18
   19 1C22              KIMMON  =       X'1C22          ; ADDRESS OF SAVE MACHINE STATE ENTRY POINT
   20 4000              K16ORG  =       X'4000          ; ADDRESS OF 16K MEMORY
   21 4000              K16SIZ  =       16384           ; SIZE OF 16 MEMORY BOARD
   22 003F              K16SGB  =       K16SIZ-1/256 ; SIGNIFICANT UPPER ADDRESS BITS FOR 16K
   23
   24                   ;       BASE PAGE DATA STORAGE
   25 0000                      .=      0
   26
   27                   ;       MAIN PROGRAM DATA STORAGE
   28
   29 0000 0000         ERRADR: .WORD   0               ; ADDRESS OF DETECTED MEMORY ERROR
   30 0002 00           ERRBTS: .BYTE   0               ; ONES REPRESENT ERROR BITS
   31 0003 00           ITCNT:  .BYTE   0               ; ITERATION COUNT
   32
   33                   ;       DATA STORAGE FOR RANDOM PATTERN TEST
   34
   35 0004 D204         RANDNO: .WORD   1234            ; RANDOM NUMBER REGISTER
   36 0006 0000         SEED:   .WORD   0               ; SAVES SEED FOR VERIFY
   37 0008 0000         ADDRCT: .WORD   0               ; DOUBLE BYTE ADDRESS COUNTER
   38 000A 0000         SCMEMA: .WORD   0               ; SCRAMBLED MEMORY ADDRESS AND ERROR ADDRES
   39
   40 000C                      .=      X'200           ; START PROGRAM CODE AT 200
   41
   42 0200 A9E0         MTEST:  LDA     #X'E0           ; INITIALIZE STACK POINTER
   43 0202 9A                   TXS
   44 0203 D8                   CLD                     ; INSURE BINARY ARITHMETIC
   45
   46                   ;       TEST: 16 PASSES WITH RANDOM DATA, PAUSE IN 16TH PASS
   47
   48 0204 A90F         MAIN10: LDA     #15             ; SET 16 ITERATION COUNT
   49 0206 8503                 STA     ITCNT
   50 0208 209402       MAIN11: JSR     RAND            ; NEW PASS, GET A RANDOM
   51 020B A504                 LDA     RANDNO          ; NUMBER IN RANDNO AND SAVE
   52 020D 8506                 STA     SEED            ; AS SEED FOR VERIFY
   53 020F A505                 LDA     RANDNO+1
   54 0211 8507                 STA     SEED+1
   55 0213 204C02               JSR     RNDGEN          ; GENERATE A RANDOM DATA PATTERN IN 16K
   56 0216 A503                 LDA     ITCNT           ; TEST IF LAST PASS
```

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K16TS K-1016 MEMORY EXERCISE
EQUATES AND DATA STORAGE

  57 0218 D011              BNE    MAIN15        ; SKIP OVER WAIT IF NOT
  58 021A A200              LDX    #0            ; WAIT FOR ABOUT 15 SECONDS IN A TIGHT LOOP
  59 021C A000      MAIN12: LDY    #0
  60 021E A921      MAIN13: LDA    #33
  61 0220 18        MAIN14: CLC
  62 0221 69FF              ADC    #-1
  63 0223 D0FB              BNE    MAIN14
  64 0225 88                DEY
  65 0226 D0F6              BNE    MAIN13
  66 0228 CA                DEX
  67 0229 D0F1              BNE    MAIN12
  68 022B A506      MAIN15: LDA    SEED          ; RESTORE RANDOM SEED FOR VERIFY PHASE
  69 022D 8504              STA    RANDNO
  70 022F A507              LDA    SEED+1
  71 0231 8505              STA    RANDNO+1
  72 0233 206902            JSR    RNDVER        ; VERIFY
  73 0236 D007              BNE    RNERLG        ; GO TO ERROR LOG IF ERROR
  74 0238 C603              DEC    ITCNT         ; DECREMENT AND CHECK ITERATION COUNT
  75 023A 10CC              BPL    MAIN11        ; LOOP UNTIL 16 ITERATIONS DONE
  76 023C 4C0402            JMP    MAIN10        ; REPEAT THE ENTIRE TEST WITH DIFFERENT
  77                                             ; DATA
  78
  79 023F 8502      RNERLG: STA    ERRBTS        ; STORE ERROR BITS
  80 0241 A50A              LDA    SCMEMA        ; STORE ERROR ADDRESS
  81 0243 8500              STA    ERRADR
  82 0245 A50B              LDA    SCMEMA+1
  83 0247 8501              STA    ERRADR+1
  84 0249 4C221C            JMP    KIMMON        ; GO TO KIM MONITOR
  85
  86                ;       RANDOM PATTERN STORED IN SCRAMBLED ORDER GENERATE ROUTINE
  87
  88 024C A900      RNDGEN: LDA    #0            ; INITIALIZE ADDRESS COUNTER
  89 024E 8508              STA    ADDRCT        ; TO 8192
  90 0250 A940              LDA    #K16SIZ/256
  91 0252 8509              STA    ADDRCT+1
  92 0254 209402    STORPH: JSR    RAND          ; GENERATE A RANDOM NUMBER
  93 0257 208202            JSR    MADDR         ; FORM A SCRAMBLED MEMORY ADDRESS
  94 025A A504              LDA    RANDNO        ; STORE A RANDOM BYTE
  95 025C A200              LDX    #0            ; INDIRECTLY THROUGH SCRAMBLED MEMORY
  96 025E 810A              STA    (SCMEMA,X)    ; ADDRESS AT SCMEMA
  97 0260 C608              DEC    ADDRCT        ; DECREMENT ADDRESS COUNTER
  98 0262 D0F0              BNE    STORPH        ; AND LOOP IF NOT ZERO
  99 0264 C609              DEC    ADDRCT+1
 100 0266 D0EC              BNE    STORPH
 101 0268 60                RTS                  ; RETURN WHEN DONE
 102
 103 .
 104                ;       RANDOM PATTERN STORED IN SCRAMBLED ORDER VERIFY ROUTINE
 105
 106 0269 A940      RNDVER: LDA    #K16SIZ/256   ; INITIALIZE ADDRESS COUNTER
 107 026B 8509              STA    ADDRCT+1
 108 026D 209402    VERFPH: JSR    RAND          ; GENERATE A RANDOM NUMBER
 109 0270 208202            JSR    MADDR         ; FORM SCRAMBLED MEMORY ADDRESS
 110 0273 A10A              LDA    (SCMEMA,X)    ; GET DATA FROM MEMORY INDIRECTLY
 111 0275 4504              EOR    RANDNO        ; THROUGH SCMEMA
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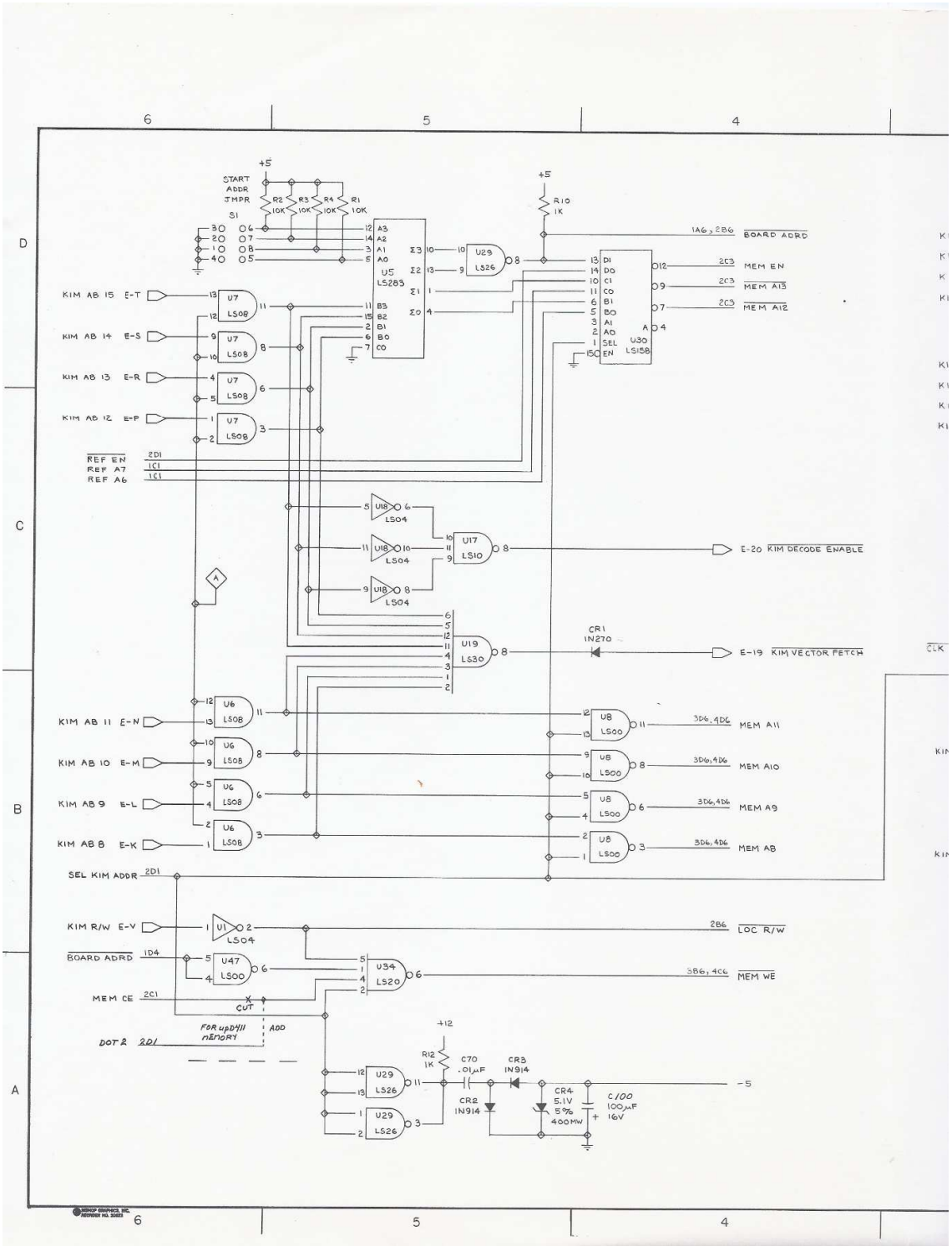
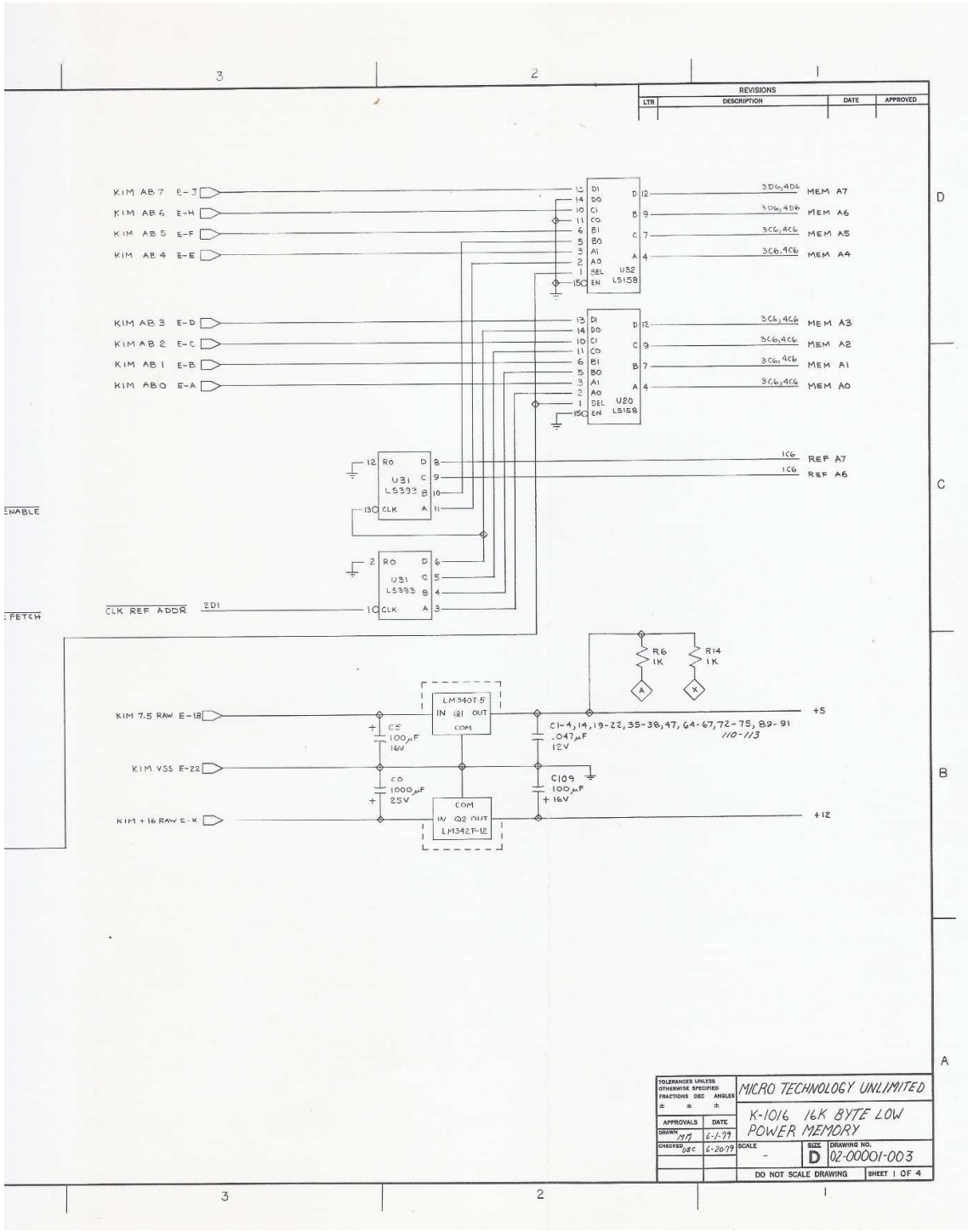
K16TS K-1016 MEMORY EXERCISE
EQUATES AND DATA STORAGE

  112 0277 D008              BNE    VERRET        ; GO RETURN ON UNEQUAL COMPARE
  113 0279 C608              DEC    ADDRCT        ; DECREMENT ADDRESS COUNTER
  114 027B D0F0              BNE    VERFPH        ; AND LOOP IF NOT ZERO
  115 027D C609              DEC    ADDRCT+1
  116 027F D0EC              BNE    VERFPH
  117 0281 60       VERRET:  RTS                  ; RETURN
  118
  119               ;        SCRAMBLED MEMORY ADDRESS FORMATION ROUTINE
  120               ;        USES ADDRCT AND SEED TO FORM A SCRAMBLED ADDRESS IN SCMEMA
  121
  122 0282 A506     MADDR:   LDA    SEED          ; GET LOWER BYTE OF RANDOM NUMBER
  123 0284 4508              EOR    ADDRCT        ; EXCLUSIVE-OR WITH LOWER ADDRESS
  124 0286 850A              STA    SCMEMA        ; LOWER BYTE OF RESULT
  125 0288 A507              LDA    SEED+1        ; GET UPPER BYTE OF RANDOM NUMBER
  126 028A 4509              EOR    ADDRCT+1      ; EXCLUSIVE-OR WITH UPPER ADDRESS
  127 028C 293F              AND    #K16SGBT      ; SAVE SIGNIFICANT BITS OF RESULT
  128 028E 18                CLC
  129 028F 6940              ADC    #K16ORG/256   ; ADD IN FIRST PAGE NUMBER OF BOARD
  130 0291 850B              STA    SCMEMA+1      ; BEING TESTED
  131 0293 60                RTS                  ; RETURN
  132
  133
  134               ;        RANDOM NUMBER GENERATOR SUBROUTINE
  135               ;        ENTER WITH SEED IN RANDNO
  136               ;        EXIT WITH NEW RANDOM NUMBER IN RANDNO
  137               ;        USES 16 BIT FEEDBACK SHIFT REGISTER METHOD
  138               ;        DESTROYS REGISTER A AND Y
  139
  140 0294 A008     RAND:    LDY    #8            ; SET COUNTER FOR 8 RANDOM BITS
  141 0296 A504     RAND1:   LDA    RANDNO        ; EXCLUSIVE-OR BITS 3, 12, 14, AND 15
  142 0298 4A                LSRA                 ; OF SEED
  143 0299 4504              EOR    RANDNO
  144 029B 4A                LSRA
  145 029C 4A                LSRA
  146 029D 4504              EOR    RANDNO
  147 029F 4A                LSRA
  148 02A0 4505              EOR    RANDNO+1      ; RESULT IS IN BIT 3 OF A
  149 02A2 4A                LSRA                 ; SHIFT INTO CARRY
  150 02A3 4A                LSRA
  151 02A4 4A                LSRA
  152 02A5 4A                LSRA
  153 02A6 2605              ROL    RANDNO+1      ; SHIFT RANDNO LEFT ONE BRINGING IN CARRY
  154 02A8 2604              ROL    RANDNO
  155 02AA 88                DEY                  ; TEST IF 8 NEW RANDOM BITS COMPUTED
  156 02AB D0E9              BNE    RAND1         ; LOOP FOR MORE IF NOT
  157 02AD 60                RTS                  ; RETURN
  158 .
  159 0000                   .END
NO ERROR LINES
```


START ADDR JMPR
S1
R2 10K
R3 10K
R4 10K
R1 10K
+5
U5 LS283
U29 LS26
R10 1K
U30 LS158
1A6, 2B6 BOARD ADRD
2C3 MEM EN
2C3 MEM A13
2C3 MEM A12
KIM AB 15 E-T
KIM AB 14 E-S
KIM AB 13 E-R
KIM AB 12 E-P
U7 LS08
REF EN 2D1
REF A7 1C1
REF A6 1C1
U18 LS04
U17 LS10
E-20 KIM DECODE ENABLE
U19 LS30
CR1 IN270
E-19 KIM VECTOR FETCH
CLK
KIM AB 11 E-N
KIM AB 10 E-M
KIM AB 9 E-L
KIM AB 8 E-K
U6 LS08
U8 LS00
3D6, 4D6 MEM A11
3D6, 4D6 MEM A10
3D6, 4D6 MEM A9
3D6, 4D6 MEM A8
SEL KIM ADDR 2D1
KIM R/W E-V
U1 LS04
2B6 LOC R/W
BOARD ADRD 1D4
U47 LS00
U34 LS20
5B6, 4C6 MEM WE
MEM CE 2C1
CUT
FOR upD411 MEMORY
ADD
DOT 2 2D1
+12
R12 1K
C70 .01μF
CR3 IN914
CR2 IN914
CR4 5.1V 5% 400MW
C100 100μF 16V
-5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KIM AB 6 E-H
KIM AB 5 E-F
KIM AB 4 E-E
KIM AB 3 E-D
KIM AB 2 E-C
KIM AB 1 E-B
KIM AB 0 E-A
U32 LS158
U20 LS158
3D6,4D6 MEM A7
3D6,4D6 MEM A6
3C6,4C6 MEM A5
3C6,4C6 MEM A4
3C6,4C6 MEM A3
3C6,4C6 MEM A2
3C6,4C6 MEM A1
3C6,4C6 MEM A0
U31 LS393
1C6 REF A7
1C6 REF A6
CLK REF ADDR
2D1
ENABLE
FETCH
R6 1K
R14 1K
KIM 7.5 RAW E-18
KIM VSS E-22
KIM +16 RAW E-X
LM340T-5
LM342P-12
C5 100µF 16V
C0 1000µF 25V
C109 100µF 16V
C1-4,14,19-22,35-38,47,64-67,72-75,89-91 .047µF 12V
110-113
+5
+12
TOLERANCES UNLESS OTHERWISE SPECIFIED
FRACTIONS DEC ANGLES
APPROVALS DATE
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MICRO TECHNOLOGY UNLIMITED
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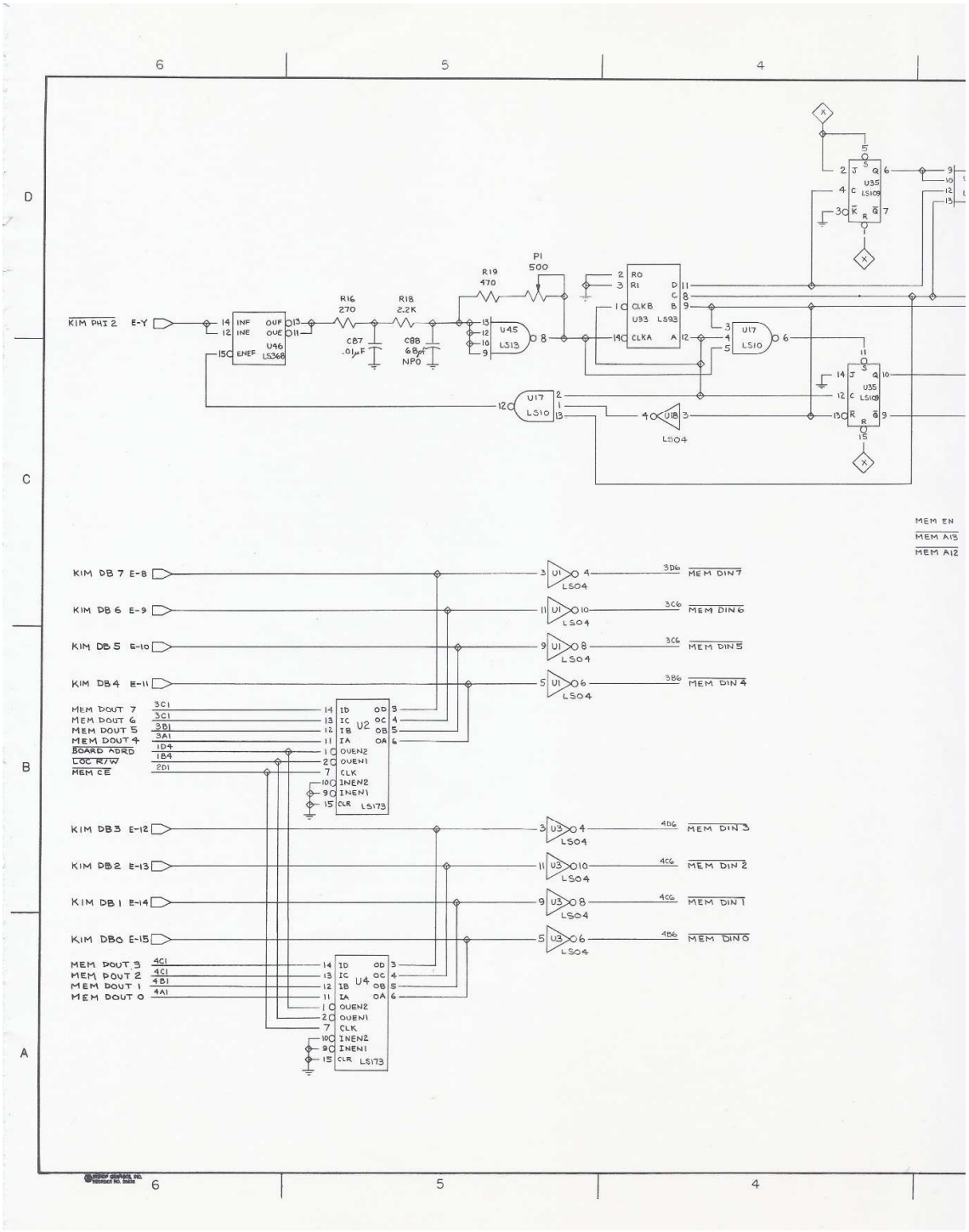
KIM PHI 2 E-Y
U46 LS368
R16 270
R18 2.2K
C87 .01μF
C88 68pf NPO
R19 470
P1 500
U45 LS13
U33 LS93
U17 LS10
U18 LS04
U35 LS109
MEM EN
MEM A13
MEM A12
KIM DB 7 E-8
KIM DB 6 E-9
KIM DB 5 E-10
KIM DB 4 E-11
KIM DB 3 E-12
KIM DB 2 E-13
KIM DB 1 E-14
KIM DB0 E-15
MEM DOUT 7
MEM DOUT 6
MEM DOUT 5
MEM DOUT 4
BOARD ADRD
LOC R/W
MEM CE
MEM DOUT 3
MEM DOUT 2
MEM DOUT 1
MEM DOUT 0
U2
U4
LS173
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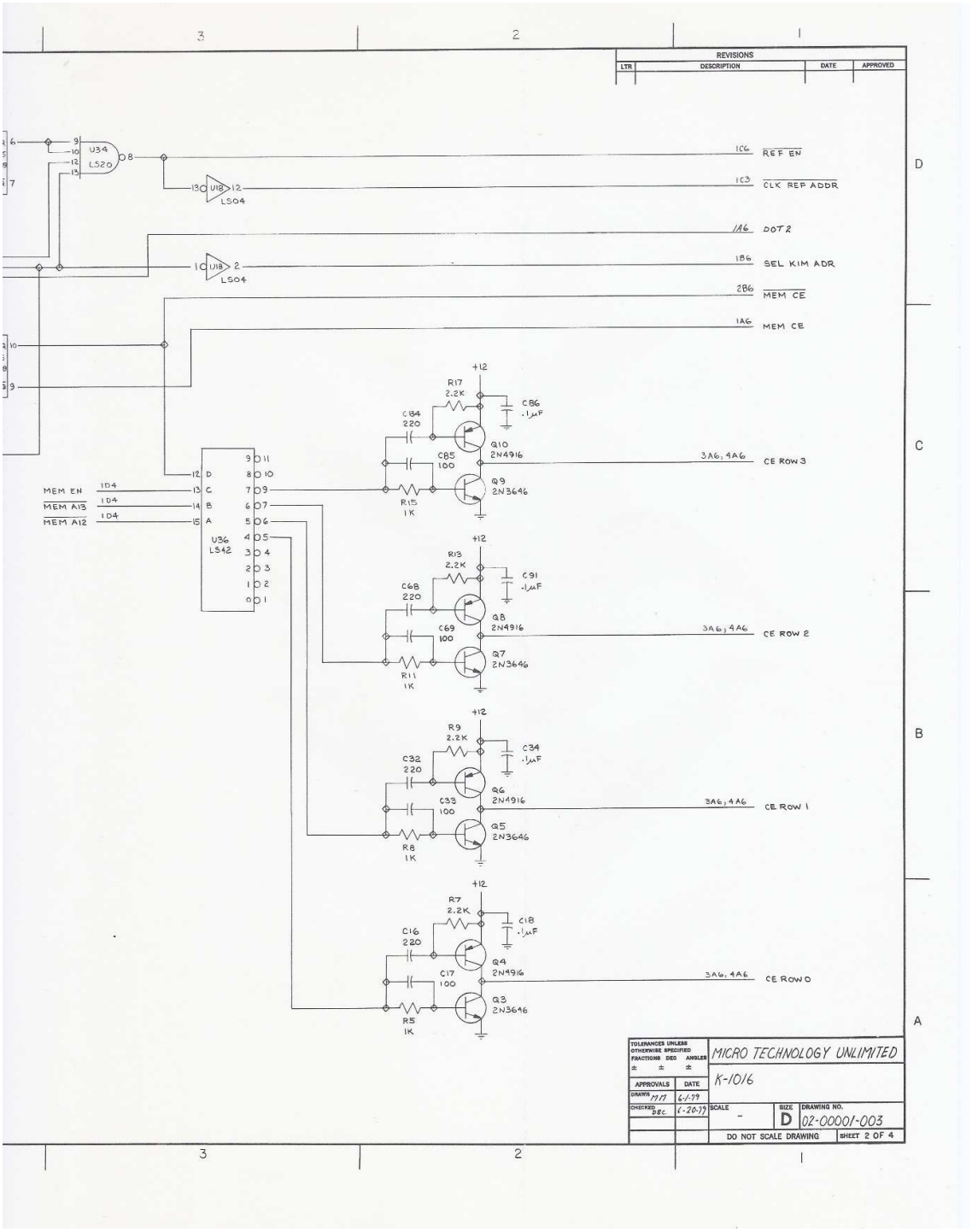
MEM DIN4
MEM DIN3
MEM DIN2
MEM DIN1
MEM DIN0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U18
LS04
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1A6 DOT 2
1B6 SEL KIM ADR
2B6 MEM CE
1A6 MEM CE
MEM EN 1D4
MEM A13 1D4
MEM A12 1D4
U36
LS42
+12
R17 2.2K
C84 220
C85 100
C86 .1μF
Q10 2N4916
Q9 2N3646
R15 1K
3A6, 4A6 CE ROW 3
R13 2.2K
C68 220
C69 100
C91 .1μF
Q8 2N4916
Q7 2N3646
R11 1K
3A6, 4A6 CE ROW 2
R9 2.2K
C32 220
C33 100
C34 .1μF
Q6 2N4916
Q5 2N3646
R8 1K
3A6, 4A6 CE ROW 1
R7 2.2K
C16 220
C17 100
C18 .1μF
Q4 2N4916
Q3 2N3646
R5 1K
3A6, 4A6 CE ROW 0
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K-1016
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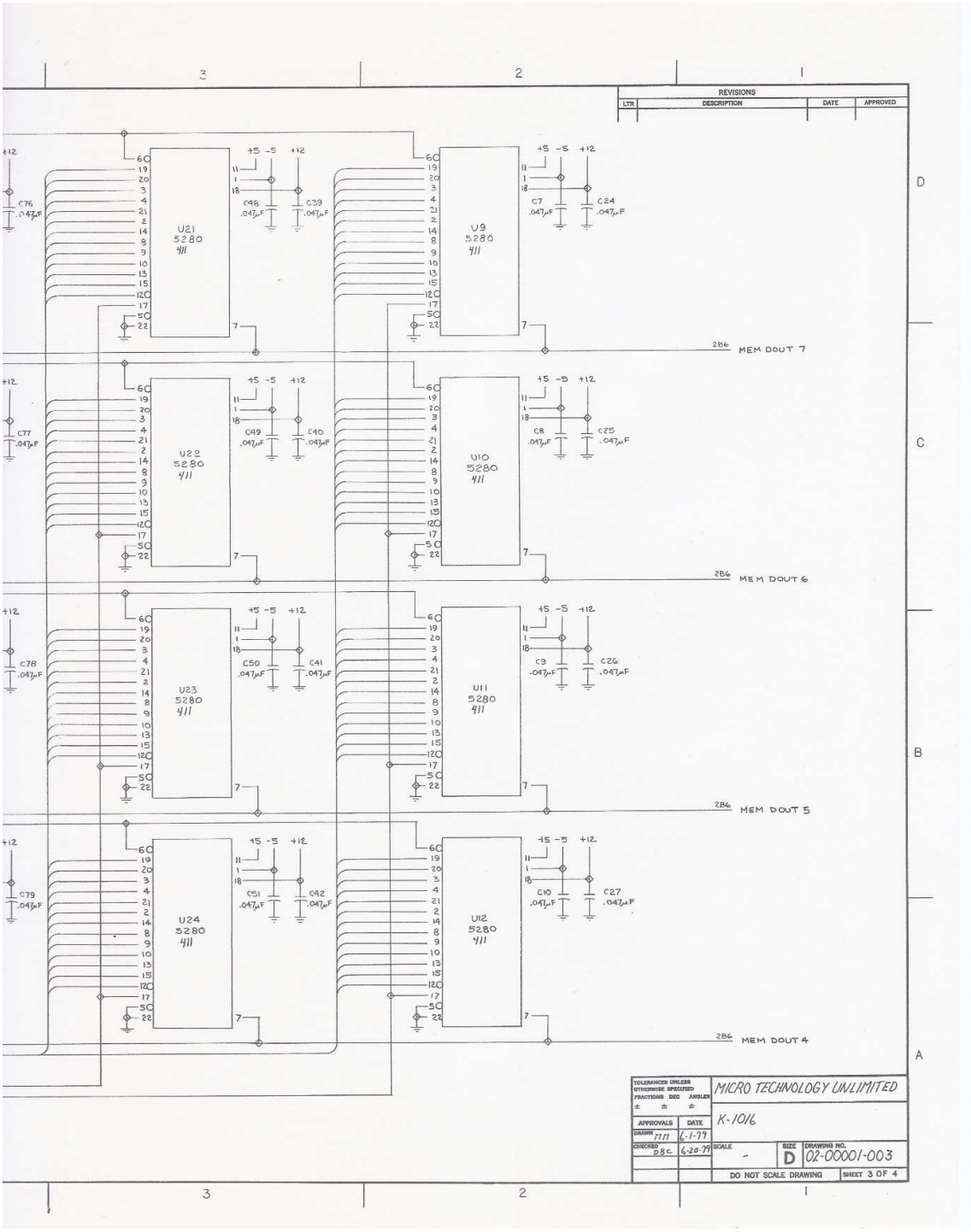
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+12
+5
-5
C76 .047μF
C77 .047μF
C78 .047μF
C79 .047μF
C48 .047μF
C39 .047μF
C7 .047μF
C24 .047μF
C49 .047μF
C40 .047μF
C8 .047μF
C25 .047μF
C50 .047μF
C41 .047μF
C9 .047μF
C26 .047μF
C51 .047μF
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C27 .047μF
286 MEM DOUT 7
286 MEM DOUT 6
286 MEM DOUT 5
286 MEM DOUT 4
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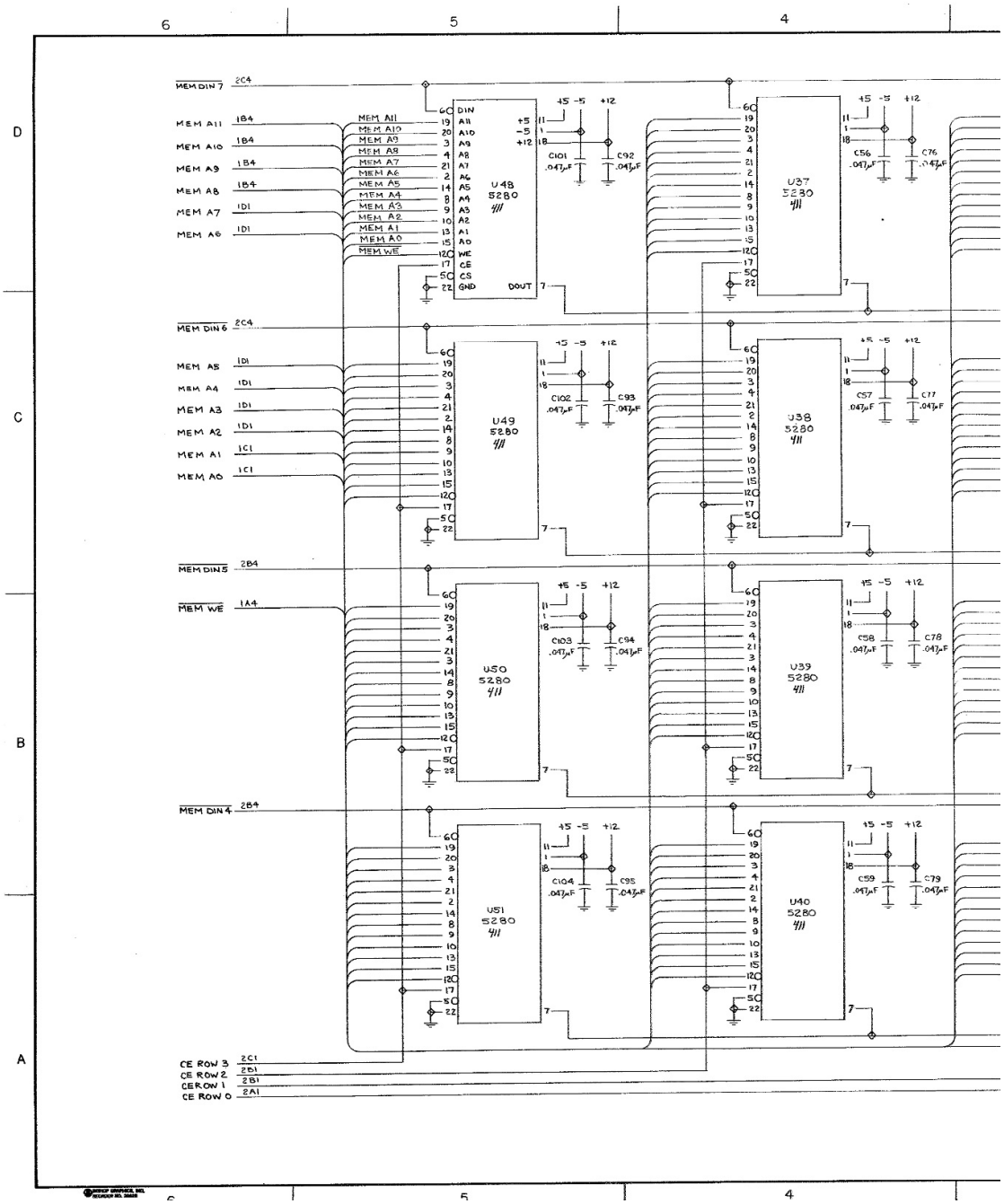
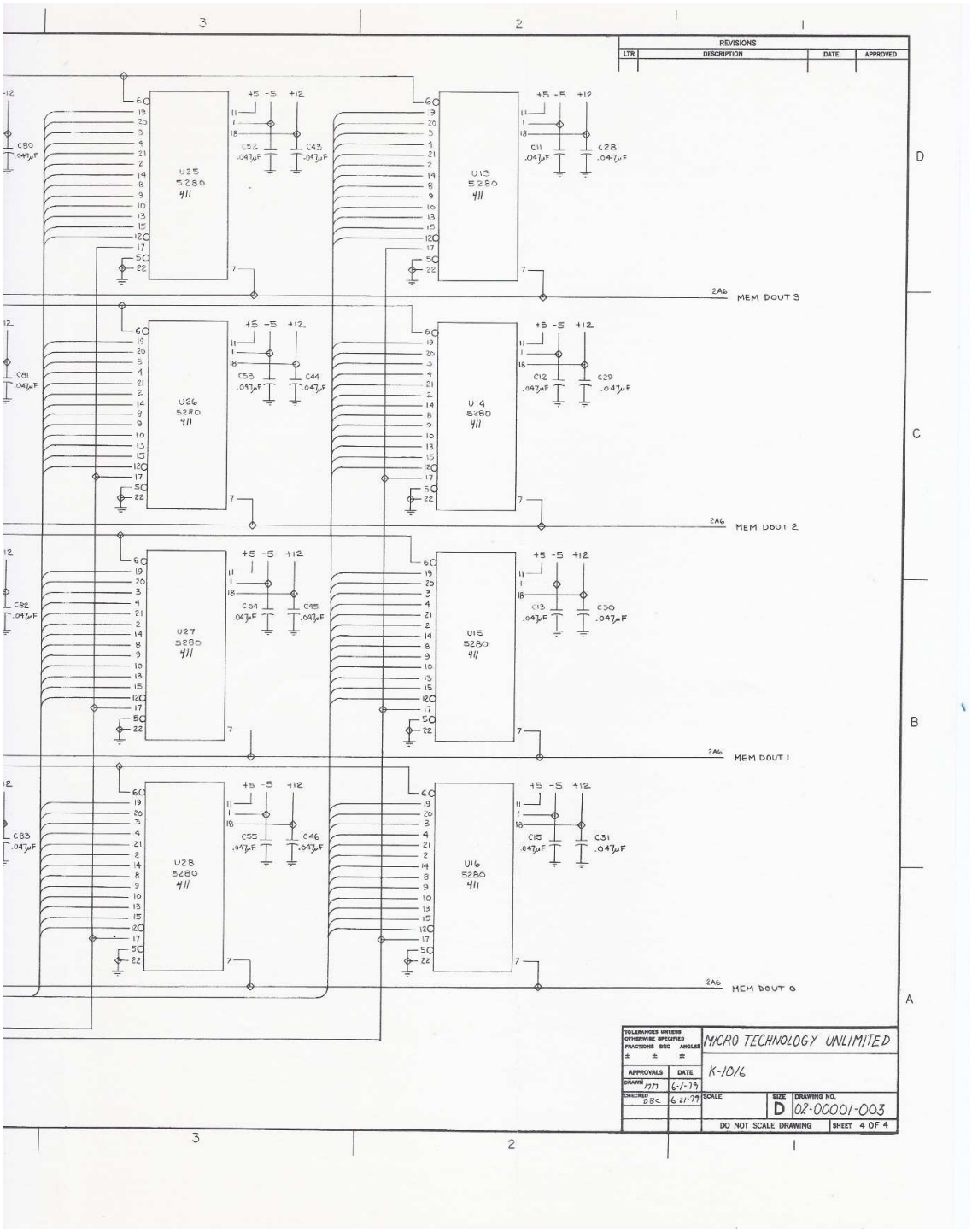

MEM DIN 7
MEM DIN 6
MEM DIN 5
MEM DIN 4
MEM WE
MEM A11
MEM A10
MEM A9
MEM A8
MEM A7
MEM A6
MEM A5
MEM A4
MEM A3
MEM A2
MEM A1
MEM A0
CE ROW 3
CE ROW 2
CE ROW 1
CE ROW 0
U48 5280 4/11
U49 5280 4/11
U50 5280 4/11
U51 5280 4/11
U37 5280 4/11
U38 5280 4/11
U39 5280 4/11
U40 5280 4/11
C101 .047µF
C102 .047µF
C103 .047µF
C104 .047µF
C92 .047µF
C93 .047µF
C94 .047µF
C95 .047µF
C56 .047µF
C57 .047µF
C58 .047µF
C59 .047µF
C76 .047µF
C77 .047µF
C78 .047µF
C79 .047µF
+5
-5
+12
GND
DOUT
DIN
WE
CE
CS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C52 .047μF
C43 .047μF
C11 .047μF
C28 .047μF
C81 .047μF
C53 .047μF
C44 .047μF
C12 .047μF
C29 .047μF
C82 .047μF
C54 .047μF
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C30 .047μF
C83 .047μF
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C31 .047μF
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2A6 MEM DOUT 2
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TOLERANCES UNLESS OTHERWISE SPECIFIED
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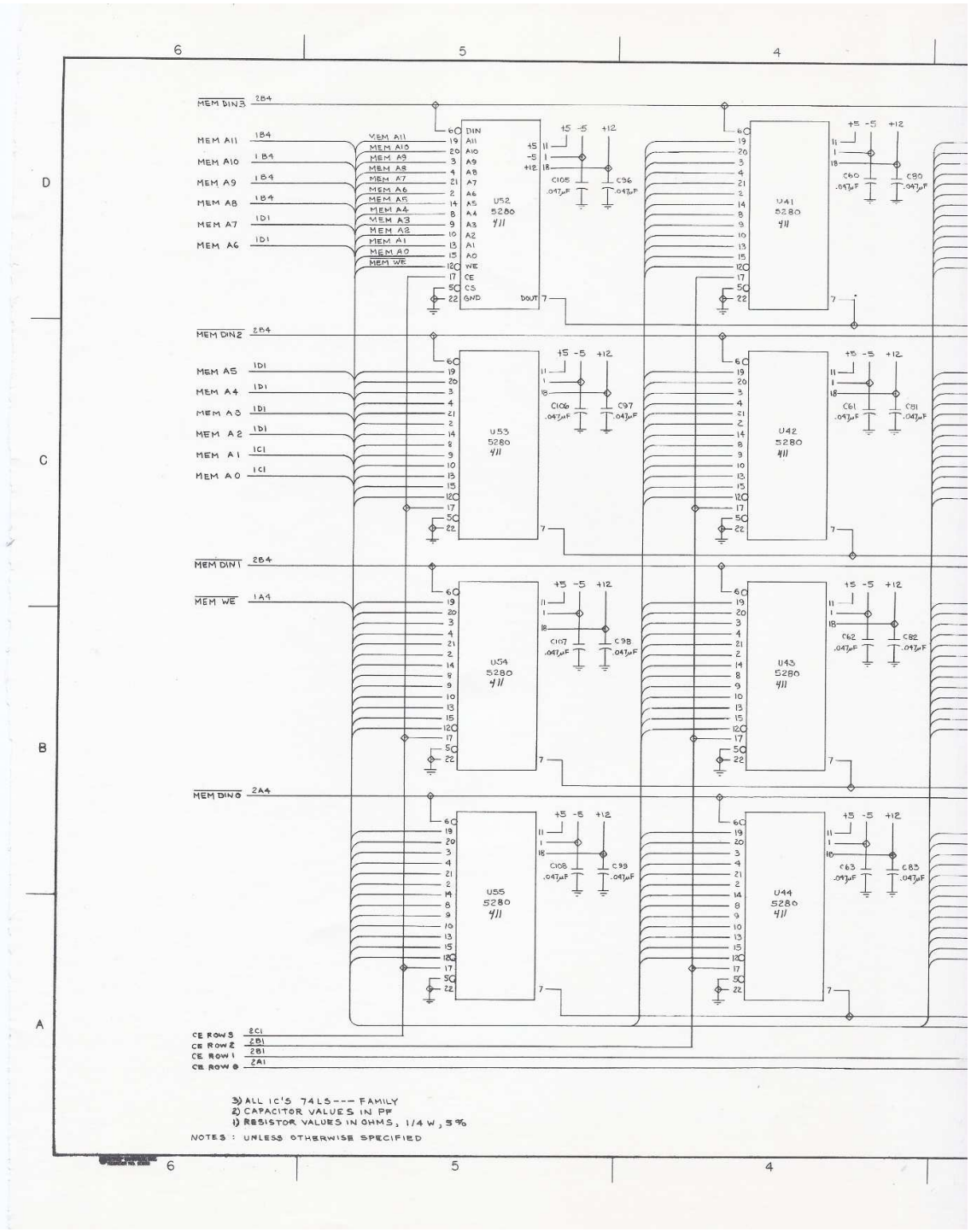

NOTES : UNLESS OTHERWISE SPECIFIED

1) RESISTOR VALUES IN OHMS, 1/4 W, 5%
2) CAPACITOR VALUES IN PF
3) ALL IC'S 74LS--- FAMILY